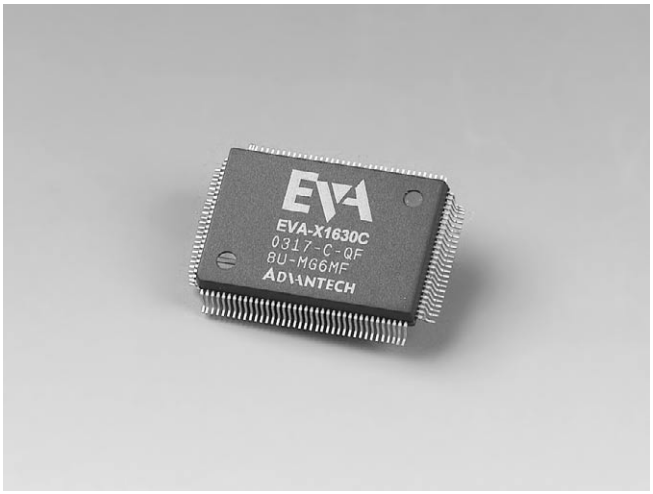
EVA-X1630C

16-bit, 75 MHz RISC Microprocessor with Ethernet and Cache



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Features

- 16-bit RISC architecture embedded microcontroller with pipeline technology
- Up to 100 MHz operating frequency
- Fast Ethernet MAC with MII interface
- Dual FIFO UART serial channels
- 80C186 software compatibility
- Up to 18 programmable I/O pins
- 128-Pin PQFP
- Compatible with 3.3 V I/O and 2.5 V core voltage
- 8K cache for I/O

Introduction

With the Ethernet protocol as the de facto “wired" network of choice for most professional, office, industrial, and even home environments, it makes sense to develop systems and leverage existing ones to take advantage of Ethernet connectivity. Advantech's EVA-X1630C integrates 10/100 Ethernet and RS-232 connectivity into an economical 80C186-compatible 75 MHz RISC microprocessor with cache and 2.5 V core voltage, making the Ethernet available to a host of applications.

The EVA-X1630C is a 16-bit, high performance, RISC architecture microprocessor with 80C186 compatibility. Additional functions integrated on the chip are: cache, SDRAM controller, non-multiplexed address bus, interrupt controller, DMA controller, timers, watchdog timer, FIFO UART serial ports, programmable I/O (PIO) pins and fast Ethernet MAC (Media AccessController).

The advanced internal high-speed local bus architecture significantly increases overall system performance. High performance plus high integration enable the EVA-X1630C to increase functionality while reducing Bill Of Materials (BOM) system costs. This, combined with a royalty-free real-time OS, contributes to its highly advantageous performance-to-cost ratio. The EVA-X1630C has been designed to meet the communication requirements of products such as device servers, medical monitors, industrial machinery, scales, security systems, code scanners, shared IP devices, thermostats, and wireless access points.

Specfications

16-bit Microprocessor

- RISC architecture with Pipeline Technology
- Five-stage pipeline
- Static design & Synthesizable design
- 1 MB memory address space
- 64 KB I/O address space
- 8K cache for I/O
- 80C186 software compatibility
- Up to 100 MHz operating frequency

SDRAM Control Interface

- Supports 16-bit data bus width
- Supports 1 Mbit x 16 and 4 Mbit x 16 SDRAM devices

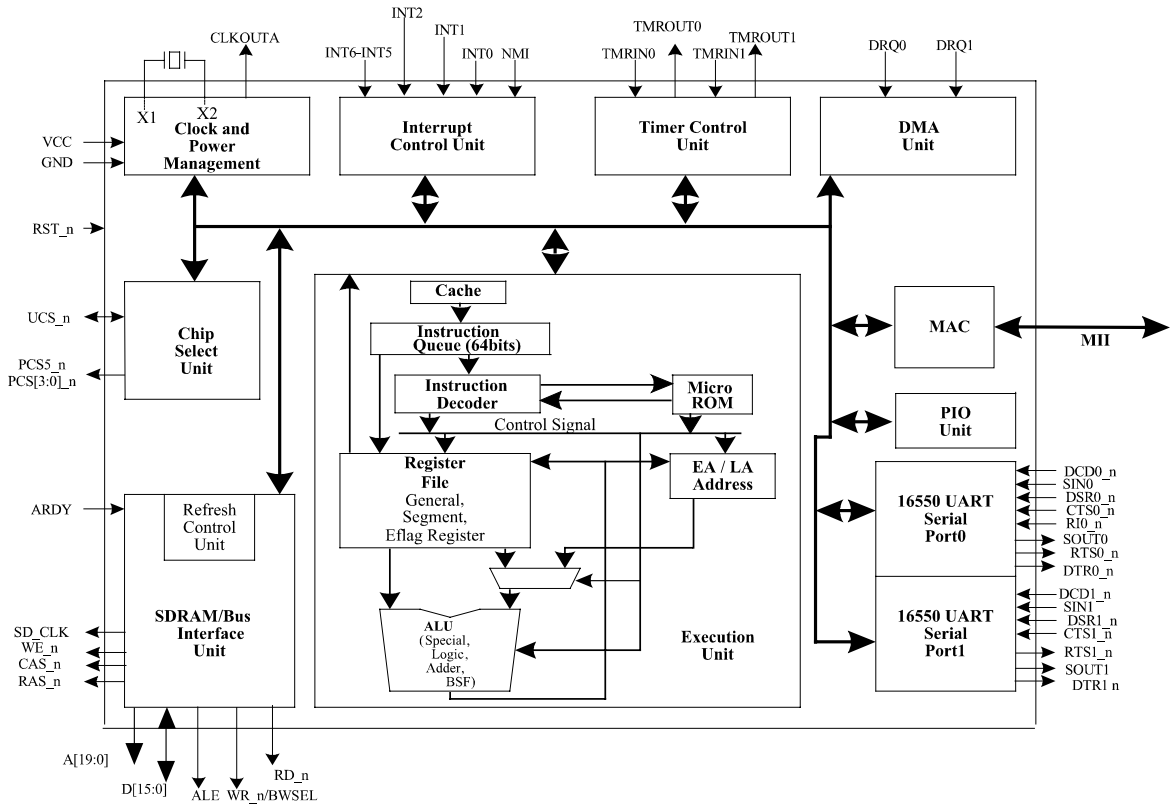
Bus Interface

- One non-multiplexed system bus interface
- Non-multiplexed address and data bus
- Supports non-multiplexed address bus A [19:0]
- 8- or 16-bit external bus dynamic access
- Supports max. 512 KB, 8- or 16-bit data width Flash ROM
- Multiplexed with SDRAM bus interface
- 64 KB I/O space
- Supports memory and I/O devices
- 1 MB memory address space
- Supports an independent bus for slower I/O devices

Supports an Independent Bus for I/O Devices

- Multiplexed address and data
- External latches are needed to separate address and data bus
- Only used for I/O devices to prevent throttling the performance of SDRAM & non-multiplexed system bus
- Shares same pins as one of the FIFO UART channels

Board Diagram



Dual FIFO UART Serial Channels

- Supports two 16550 UART serial channels with 16 bytes FIFO
- Programmable baud rate generator
- The character options are programmable for start bit, stop bit, even/odd or no parity, 5 ~ 8 data bits
- One of the FIFO UART channels shares same pins as independent I/O bus interface

1-Port Fast Ethernet MAC Ports with MII Interface

- IEEE 802.3, 802.3u specification compliant 10/100 Mbps data transfer rate
- IEEE 802.3u compliant MII interface with serial management interface
- Full-duplex/half duplex operations
- Flow control for full-duplex operations
- VLAN Supported
- Automatic CRC append and check
- Multicast/Broadcast address recognition
- Provides loop back path on the MII interface

Interrupt Controller

- Provides five maskable external interrupts
- Provides one non-maskable external interrupt

Ordering Information

▪ **EVA-X1630C**	16-bit, 75 MHz RISC microprocessor with Ethernet and cache
▪ **EVA-X1630C-DK1**	Development kit based on EVA-1630C